What is claimed is:

1. A semiconductor integrated circuit device comprising:

a MOS capacitor, one end of which is connected to a power source wire for supplying a power source voltage, and another end of which is connected to a ground potential wire for supplying a ground potential;

a ground terminal, to which said ground potential wire is connected; and

an electrostatic protection element connected in parallel with said MOS capacitor between said ground terminal and said MOS capacitor;

wherein, a wire resistance of said ground potential between a connection point on said ground wire with one end of said electrostatic protection element and said ground terminal is larger than a wire resistance of said ground potential wire between said connection point on said ground potential wire with one end of said electrostatic protection element and a connection point on said ground potential wire with the other end of said MOS capacitor.

2. A semiconductor integrated circuit device comprising:

an electrostatic protection element, one end of which is connected to a power source wire for supplying a power source voltage, and another end of which is connected to a ground potential wire for supplying a ground potential;

a ground terminal, to which said ground potential wire is connected; and

a MOS capacitor connected in parallel with said electrostatic protection element between said ground terminal and said electrostatic protection element ;

wherein, a wire resistance of said ground potential between a connection point on said ground wire with one end of said MOS capacitor and said ground terminal is larger than a wire resistance of the ground potential wire between said connection point on said ground potential wire with one end of said MOS capacitor and a connection point on said ground potential wire with the other end of said electrostatic protection element.

3. A semiconductor integrated circuit device according to any one of claims 1 ~~and~~ or 2, wherein no other diffusion layer except said electrostatic protection element is connected on said ground potential wire between said ground terminal and the connection point on said ground potential wire with one end of the MOS capacitor.

4. A semiconductor integrated circuit device comprising:

an input/output terminal;

a first electrostatic protection element, one end of which is connected to said input/output terminal and another end of which is connected to a ground potential wire for supplying the ground potential;

a MOS capacitor, one end of which is connected to a power source wire for supplying the power source voltage and another end of which is connected to the ground potential wire; and

a second electrostatic protection element connected in parallel with said MOS capacitor between said first electrostatic protection element and said MOS capacitor;

wherein a wire resistance of the ground potential wire between the connection point on the ground potential wire with the other end of said first electrostatic protection element and the connection point on the ground potential wire with one end of said second electrostatic protection element is larger than a wire resistance of the ground potential wire between the connection point on the ground potential wire with one end of said second electrostatic protection element and the connection point on the ground potential wire with the other end of said MOS capacitor.

5. A semiconductor integrated circuit device comprising:

an input/output terminal;

a first electrostatic protection element, one end of which is connected to said input/output terminal and another end of which is connected to a ground potential wire for supplying the ground potential;

a second electrostatic protection element one end of which is connected to said input/output terminal and another end of which is connected to a ground potential wire for supplying the ground potential; and

a MOS capacitor connected in parallel with said second electrostatic protection element between said first electrostatic protection element and said second electrostatic protection element ;

wherein a wire resistance of the ground potential wire between the connection point on the ground potential wire with the other end of said first electrostatic protection element and the connection point on the ground potential wire with one end of said MOS capacitor is larger than a wire resistance of the ground potential wire between the connection point on the ground potential wire with the one end of said MOS capacitor and the connection point on the ground potential wire with the other end of said second electrostatic protection element.

6. A semiconductor integrated circuit device according to any one of claims 4 ~~and~~ or 5, wherein no other diffusion layer except said first electrostatic protection element is connected on said ground potential wire between the connection point on the ground potential wire with the other end of said first electrostatic protection element and the connection point on said ground potential wire with one end of the MOS capacitor.

7. A semiconductor integrated circuit device according to any one of claims 4 ~~and~~ or 5, comprising:

a first and second commonly connected ground potential wires for supplying a ground potential and an input/output terminal;

an electrostatic protection element, one end of which is connected to said input/output terminal and another end of which is connected to said first ground potential wire; and

a MOS capacitor, one end of which is connected to the power source wire for supplying the power source voltage and another end of which is connected to said second ground potential wire;

wherein, said second ground potential wire is not connected to the input/output terminal and a diffusion layer is connected to said second ground potential wire between said ground terminal and the connection point on said second ground potential wire with the other end of said MOS capacitor.

8. A semiconductor integrated circuit device according to any one of claims 1 ~~and~~ or 2, wherein said power source wire is connected to the power source terminal, to which a predetermined power source voltage is supplied.

9. A semiconductor integrated circuit device according to any one of claims 1 ~~and~~ or 2, wherein said power source wire is connected to the power source terminal, to which a first power source voltage is supplied, through a power source conversion circuit for converting said first power source voltage.

10. A semiconductor integrated circuit device according to any one of claims 1 ~~and~~ or 2, wherein said electrostatic protection element clamps a voltage

applied to both terminals at a clamp voltage, which is lower than the dielectric breakdown voltage of said MOS capacitor.

11. A semiconductor integrated circuit device according to any one of claims 4 ~~and~~ 5, wherein said second electrostatic protection element clamps a voltage applied to both terminals at a clamp voltage, which is lower than the dielectric breakdown voltage of said MOS capacitor.

12. A semiconductor integrated circuit device according to any one of claims 1 ~~and~~ 2, wherein said electrostatic protection element is a MOS field effect transistor, the drain of which is connected to said power source wire, and the source and the drain of which are connected to said ground potential wire.

13. A semiconductor integrated circuit device according to any one of claims 4 ~~and~~ 5, wherein said second electrostatic protection element is a MOS field effect transistor, the drain of which is connected to said power source wire, and the source and the drain of which are connected to said ground potential wire.

14. A semiconductor integrated circuit device according to any one of claims 1 ~~and~~ 2, wherein said electrostatic protection element is a bipolar transistor, constituted by forming on a substrate having a first conductive type two diffusion layers having a second conductive type, an opposite conductive type

to the first conductive type, so as to closely face each other.

15. A semiconductor integrated circuit device according to any one of claims 4 ~~and~~ 5, wherein said second electrostatic protection element is a bipolar transistor, constituted by forming on a substrate having a first conductive type two diffusion layers having a second conductive type, an opposite conductive type to the first conductive type, so as to closely face each other.

16. A semiconductor integrated circuit device according to any one of claims 1 ~~and~~ 2, wherein said electrostatic protection element is a thyristor, constituted by forming on a substrate having a first conductive type two diffusion layers respectively having a first conductive type and a second conductive type, an opposite conductive type to the first conductive type, so as to closely face each other, and by further forming on a well having the second conductive type formed on said substrate having the first conductive type two diffusion layers respectively having the first conductive type and the second conductive type, so as to closely face each other.

17. A semiconductor integrated circuit device according to any one of claims 4 ~~and~~ 5, wherein said second electrostatic protection element is a thyristor, constituted by forming on a substrate having a first conductive type two diffusion layers respectively having a first conductive type and a second conductive type, an opposite conductive type to the first conductive type, so as

to closely face each other, and by further forming on a well having the second conductive type formed on said substrate having the first conductive type two diffusion layers respectively having the first conductive type and the second conductive type, so as to closely face each other.

18. A semiconductor integrated circuit device according to any one of claims 1 ~~and~~ or 2, wherein said electrostatic protection element is a diode, constituted by forming on a substrate or a well having a first conductive type two diffusion layers having a second conductive type, an opposite conductive type to the first conductive type, so as to closely face each other.

19. A semiconductor integrated circuit device according to any one of claims 4 ~~and~~ or 5, wherein said second electrostatic protection element is a diode, constituted by forming on a substrate or a well having a first conductive type two diffusion layers having a second conductive type, an opposite conductive type to the first conductive type, so as to closely face each other.